REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-6, 25-26. Specifically, the Office Action rejected claims 1-6 under 35 U.S.C. 102(e), as being anticipated by Jain et al. (U.S. 6,376,371). The Office Action also rejected claims 25 under 35 U.S.C. 103(a) as being unpatentable over Jain in view of Lien (U.S. 5,723,822) and also rejected claim 26 under 103(a) as being unpatentable over Jain in view of Joshi (US 5,955,781). Applicants have amended claims 1, 4 and added claims 27-28 to improve clarity. After entry of the foregoing amendments, claims 1-6, 25-28 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the 35 U.S.C. 102(e) rejection of claims 1-6 because Jain et al. (US Patent No. 6,376,371) does not teach every element recited in these claims.

The present invention is in general related a bonding pad structure as claims 1 and 4 recite:

1. A boding pad structure, comprising:
a copper interconnect structure having multi-layer interlevel dielectric layers and copper interconnects in the multi-layer interlevel dielectric layers;
a passivation layer over the copper interconnect structure having a pad window to expose a portion of the copper interconnects;
a barrier layer conformal to a profile of the pad window; and
an aluminum pad located in the pad window, wherein the aluminum pad is exposed by the passivation layer and is only deposited inside the pad window.

Independent claim 4 states:

4. A bonding pad structure, comprising:
a copper interconnect structure having multi-layer interlevel dielectric layers and copper interconnects in the multi-layer interlevel dielectric layers;

a passivation layer over the copper interconnect structure having a pad window to expose a portion of the copper interconnects;

a barrier layer conformal to a profile of the pad window and extended along a portion of the surface of the passivation layer surrounded the pad window; and

an aluminum pad located over the barrier layer, wherein the aluminum pad is disposed only inside the pad window and over a portion of the surface of the passivation layer surrounding the pad window.

Jain discloses a method of forming a refractory metal nitride and a refractory metal silicon nitride layer by using MOCVD. Since these layers can be formed at wafer temperature lower than 400℃ with relatively small amounts of carbon within the film, the layers can be formed relatively conformal and has reasonably good diffusion barrier properties (See ABSTRACT).

The Office Action regards Jain's the layer 56 as the passivation layer, and Jain's layer 66 as the aluminum layer as claimed in the present invention. However, in fact, the layer 56 is an interlevel dielectric layer (col. 5, lines 35-44) that functions to electrically insulate conductive elements. Hence, the layer 56 in Jain's reference is not a passivation layer for bonding process after all interconnect structures are completely formed. Moreover, the layer 66 is a conductive layer overlaying the second interlevel dielectric layer. The combination of layers 64, 66 formed a bit line 66 (col. 5, lines 48-54). Furthermore, after the bit line 66 is formed, a passivation layer 72 is deposed overlying the second inerlevel dielectric layer (col. 5, lines 55-57). Hence, the layer 66 is part of the interconnect structure and is not an aluminum pad formed over the interconnect structure. Applicants also claim the aluminum pad is exposed by the passivation layer (as described in claim 1), but in Jain's reference, the layer 66 is covered by the passivation layer 72 and can not be exposed for connecting with bonding wires or solder balls. Besides, Applicants claim the aluminum pad is disposed inside the pad window only (claim 1) or inside the pad window and over a portion of the surface of the passivation layer surrounding the pad window (claim 4). However, in Jain's reference, the layer 66 and 64 formed a bit line 62, and the layer 62 is not formed only inside a pad window, or only inside a pad window and over a portion

of the surface of the passivation layer surrounding the pad window, as required by claims 1 and 4 , respectively.

Thus, Jain fails to teach each and every element of claims 1 and 4, and claims 1 and 4 are not anticipated by and are patentable over Jain's reference.

For at least the same reasons, dependent claims 2-3, 5-6 are not anticipated by and patently define over the prior art as well.

Applicants respectfully traverse the rejection of claim 25 under 103(a) as being unpatentable over Jain in view of Lien (U.S. 5,723,822) and also respectfully traverse the rejection of claim 26 under 103(a) as being unpatentable over Jain in view of Joshi (US 5,955,781).

To provide the missing element in Jain, Lien is cited to teach an aluminum pad located in the pad window is connected to a bonding wire, and Joshi is cited to teach an aluminum pad located in the pad window is connected to a solder ball. However, neither Lien nor Joshi can cure the deficiencies of Jain as discussed above. Thus, claims 1 and 4 as well as their dependent claims 2-3, 5-6, and 25-26 are patentable over Jian, Lien and Joshi.

Furthermore, Lien discloses a structure comprising a bonding pad 116, a passivation layer 109 exposes a portion of the bonding pad 116, and a bonding wire 114. The Office Action considers it is obvious to modify the structure of Jain to include the bonding wire of Lien. If combined, Jain and Lien do not achieve the invention of claim 25 because Jain discloses the interconnect structure and Lien suggests the bonding wire. If Jian and Lien were combined as proposed, a semiconductor device having interconnect structure comprising metal layer 36, interlevel dielectric layer 56 and bit line 62 (as described in Jain's reference) and a bonding structure comprising a bonding pad 116, passivation layer 109 and a bonding wire 114 (as described in Lien's reference) is obtained. Therefore, the combination of Jain and Lien would dissuade one of ordinary skill in the art from arriving at the present invention of claim 25.

Joshi discloses a structure comprising a bonding pad 248, a passivation layer exposes a portion of the bonding pad 248, and a solder ball 208. If combining Jian and Joshi, a

semiconductor device having interconnect structure comprising metal layer 36, interlevel dielectric layer 56 and bit line 62 (as described in Jain's reference) and a bonding structure comprising a bonding pad 248, passivation layer and a solder ball 208 (as described in Joshi's reference) is obtained. Hence, Jain and Joshi do not achieve the invention of claim 26.

For at least the foregoing reasons, Applicants respectfully submits that claims 25 and 26 patently define over the prior art references, and should be allowed.

Applicants further newly added dependent claims 27-28 of claim 4 reciting the aluminum pad located in the pad window is connected with a bonding wire and a solder ball respectively.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-6, 25-28 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809